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Novel Asymmetric Hybrid 15 Level Inverter with Reduced Number of Switches Using Different PWM Techniques – Part II (Hardware Studies)

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Abstract: This paper presents a new asymmetric cascaded H-bridge Multi Level Inverter (MLI) with less number of power devices for industries and renewable energy applications. Cascaded MLI are more popular in electric utilities and industrial drives. MLI reduces Total Harmonic Distortion (THD) present in the output voltage. MLI performance is very good on the higher value of voltage apply to the drive. The cascaded H-bridge inverters are classified based on the input supply voltage from the unequal sources like symmetric and asymmetric inverter. The proposed topology consists of one H-bridge (with 4 switches) and full bridge unit (with 3 switches) for 15 level output voltage. In this paper THD is reduced to 3.23% by using SPWM technique. THD analysis is calculated by FFT spectrum of output waveforms using MATLAB/SIMULINK. The proposed topology is verified through the prototype hardware of single phase 15 level hybrid asymmetric inverter using FPGA based Xilinx SPARTAN 3E processor. These processors provide proper gating signals for switches using SPWM application.

Keywords: Asymmetric Multilevel inverter (AMLI), Total Harmonic Distortion (THD), PWM methods.

I. INTRODUCTION

MLI were successively introduced in 1975. The MLI basically started with the 3-level inverter. The idea of a MLI is to achieve high power with series of semiconductor switches, small amount of lower voltage DC sources to carry out the power conversion by synthesizing a stepped voltage output [1]. The DC voltage supplies are consists of batteries and renewable energy sources. In order to achieve high voltage at the output stage commutation power switches are used. These power switches depends on the connected DC voltage source rating value [2].

This paper essentially focused on AMLI (asymmetric multilevel inverter) with less number of power switches to produce 15-level output with less number of DC sources. AMLI is chosen over the symmetric one because it requires least number of switches to get the 15-level voltage waveform. AMLI consists of unequal voltage source compare to SMLI, the SMLI have equal value of voltage sources that all are different. The essential output waveform is obtained by giving appropriate switching pulses to the gate driver circuits. In this proposed AMLI mainly discuss of hybrid modulation technique are briefly verified [3] [4]. For this analysis, POD base hybrid modulation technique is developed and explored. The performance parameters for POD techniques theoretically analysis and computed.

II. BASIC OPERATIONS OF AMLI

This topology introduces the main idea of using unequal DC source to produce an AC sinusoidal output voltage waveform. Every H-bridge inverter unit is coupled with DC source. Based on this condition this topology eliminates the clamping diodes from the MLI diode clamping and flying capacitor required ML flying capacitors inverter. AMLI have different DC voltage sources. In cascade harvest voltage of H-bridge inverter produced a sinusoidal stepped output waveform. The summing of all H-bridge required the output voltage, and this voltage produces N number of H-bridges. In this method 12 switches and 3 DC different voltage source involved to generate the 15-level output voltage waveform [5][6].

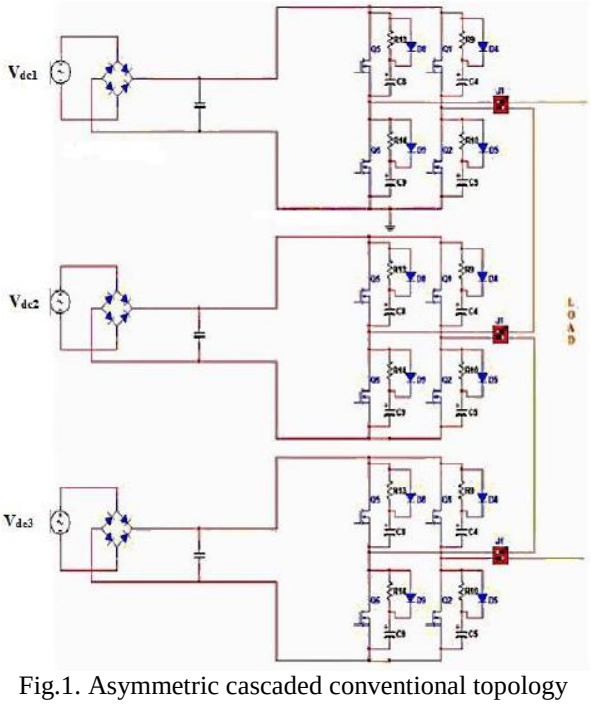

Fig.1. Asymmetric cascaded conventional topology

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III. MODIFIED ASYMMETRI MULTILEVEL INVERTER

In this proposed modified AMLI topology as shown in below Fig.2. It has 7 switches and 3 DC unequal voltage sources are V_{dc1}, V_{dc2}, V_{dc3}, these voltages are used to produce 15-level output voltage [7].The output voltage of 15-level inverter is represent in the below Fig.2. The open and close switches are S_1, S_2, S_3 these switches are operated on ON and OFF mode. The conduction of these switches connected based on positive, negative, and zero voltage to withstand the output voltage. When all switches are turned OFF the obtained output voltage is zero. The conduction switches are connected in upper leg and lower leg in the H-bridge unit. Remaining voltage is achieved by proper switching between the other switches. The switching pattern tabulated in Table 1.In full bridge inverter part turned on for 2 switches one from upper part and remaining switch is lower part from the output voltage. When S_4 and S_5 are turned ON positive output voltage is produced, when the switches S_6 and S_7 closed negative output voltage is produced. The method of a pulse generation circuit topology differs from the other unit. So we have to get the accurate pulse pattern to fire the switches at the particular instant. In this circuit unidirectional switches are used to reduce the minimum switches, harmonics are reduced to generate the fifteen levels and reduction of switches avoid switching losses [8]-[9]

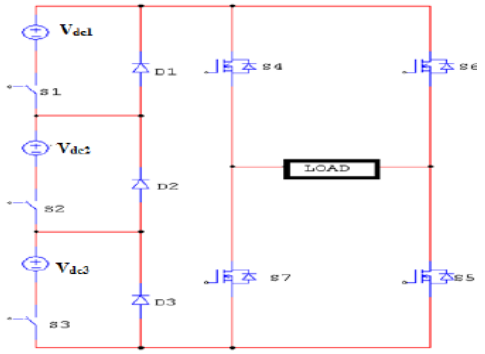

Fig.2. Proposed AMLI topology

Table.1. Switching pattern for asymmetric unit and H-bridge unit of modified AMLI

SWITCHES							Output Voltage
Asymmetric Unit Switches			H-Bridge Switches				
S1	S2	S3	S4	S5	S6	S7	
1	0	0	1	1	0	0	V_{dc1}
0	1	0	1	1	0	0	V_{dc2}
1	1	0	1	1	0	0	$V_{dc1}+V_{dc2}$
0	0	1	1	1	0	0	V_{dc3}
1	0	1	1	1	0	0	$V_{dc1}+V_{dc3}$
0	1	1	1	1	0	0	$V_{dc2}+V_{dc3}$
1	1	1	1	1	0	0	$V_{dc1}+V_{dc2}+V_{dc3}$
0	0	0	0	1	1	0	0
1	0	0	0	0	1	1	V_{dc1}
0	1	0	0	0	1	1	V_{dc2}
1	1	0	0	0	1	1	$V_{dc1}+V_{dc2}$
0	0	1	0	0	1	1	V_{dc3}
1	0	1	0	0	1	1	$V_{dc1}+V_{dc3}$
0	1	1	0	0	1	1	$V_{dc2}+V3$
1	1	1	0	0	1	1	$V_{dc1}+V_{dc2}+V_{dc3}$

IV. DESIGN AND IMPLEMENTATION OF AMLI

The proposed system design and specification of the variety of hardware equipments of the AMLI are discussed. It includes a asymmetric source with switches, single phase H-bridge inverter, and freewheeling diodes. This modified proposed system has more beneficial compare to other topologies. This system requires least number of semiconductor power switches and power diodes.

The AMLI is works in open- loop arrangement. Opto-coupler is isolated by an control method and power stage these are consist by inverters. The opto-coupler and FPGA controller are supplied by the transformer. The transformer is supplied by single phase 230V AC source. The control stage consists of FPGA controller that has been program to provide PWM pulses that drives the MOSFET switches. The DC supply voltage from the renewable energy sources is connected to the inverter circuit. Resistive load is connected across output terminals of the MLI. The opto coupler input is given to the PWM pulse driver to generate the proper pulses. Opto-coupler TLP 250 is used to drive the MOSFETs.

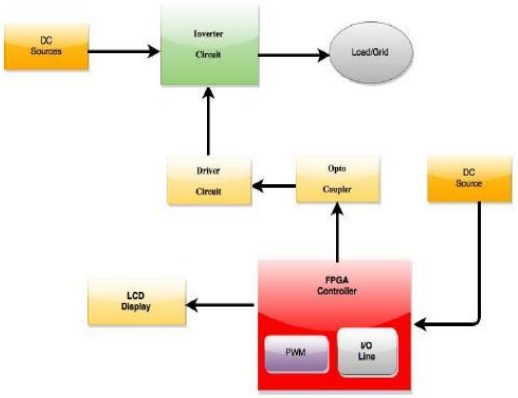

Fig.3. Block diagram design of AMLI

A.TECHNICAL SPECIFICATIONS

The technical specifications of the proposed AMLI are as tabulated in table 2.

Table.2. Technical specifications of AMLI

Sl.No.	Parameter	Specifications
1	DC voltage sources	5V, 10V, 20V
2	Switching frequency	10 kHz
3	Output voltage	+33V
5	Power output	45 W
7	Modulation technique	Hybrid modulation
8	PWM Controller	Spartan 3E

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V. MODULATION METHODS OF AMLI

In order to get the enhanced output voltage, quality output, and appropriate modulation method must be suitable for the modified MLI. This paper discusses about different modulation technique among the novel hybrid modulation strategy is used to compact the switching losses and less harmonic stuffing in the higher harmonic order to obtain the output waveform. PODPWM gives quality output and higher output voltage with less THD 5% compare to different hybrid modulation schemes involved in the proposed AMLI. FPWM technique is utilized for full bridge inverter and carrier PWM methods are used for asymmetric basic part switches. In order to reduce the THD, POD technique is used. POD strategy improves the performance of the inverter. It is suitable method to reduce the harmonics, switching loss.

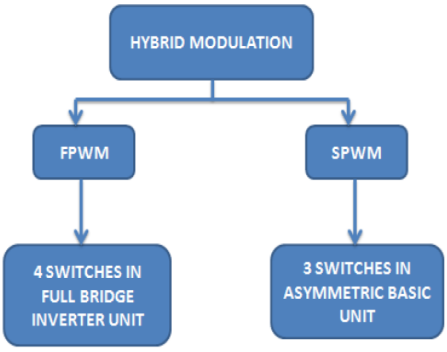

Fig.4. Block diagram of hybrid PWM modulation

A. FLOW CHART

This flow chart is developed to generate a PWM pulses . this flow chart analysis was done by using VHDL language. Using this progrmme FPGA download the programe into the chip. this chip is to provide the PWM pulses to necessary to drive the gate terminal of the switch.

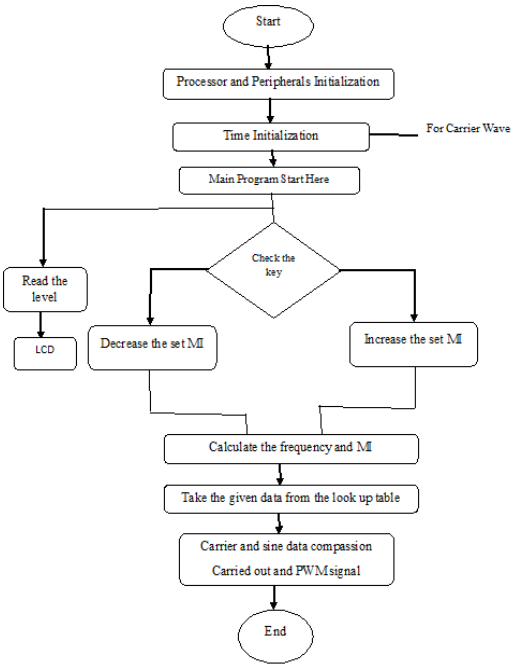

Fig.5. Flow chart for generating hybrid PWM pulses from the FPGA controller

VI. HARDWARE IMPLEMENTATION AND RESULT ANALYSIS

In this paper hardware execution and experiment investigational results are presented. The hardware connections and system organization are explained and the THD analysis is done.

A. EXPERIMENTAL SETUP

Asymmetric multilevel inverter experimental hardware components setup as shown in below Fig.6. it contains more number of power supply unit, inverter stage, and controller unit as shown in the setup experimental hardware.

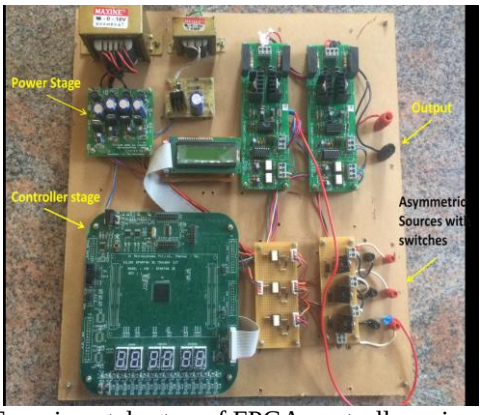

Fig.6.Experimental setup of FPGA controller using AMLI

A 230 V AC Single phase supply has given to the step down transformer. The 230V input AC is stepped down transformer 9V and 18V and this voltage is given to the bridge rectifier circuit it is converts AC to DC. Capacitors are used to filter the rectifier output waveform. FPGA controller is used to generate the PWM signals. Generated signals are transferred to the input of the opto-isolator driver circuit. It drives the MOSFET switch to get the 15-level of output voltage waveform.

The hardware model of the AMLI is as shown in Fig.7. Input DC voltages are 5V, 10V and 20V, the output voltage obtained is 33.1V

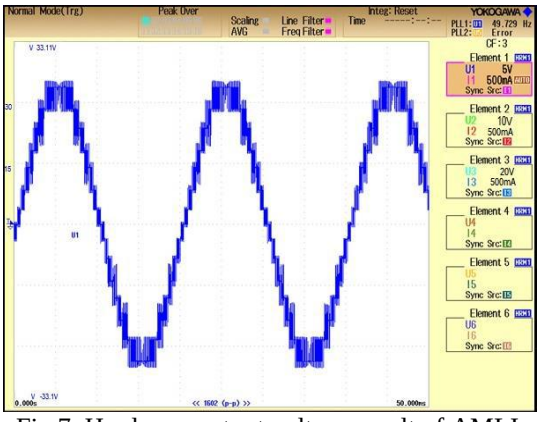

Fig.7. Hardware output voltage result of AMLI

Fig.8. Shows the hardware output current and voltage results of AMLI. The voltage and current are establish to the phase .the obtained current output is 1.52A

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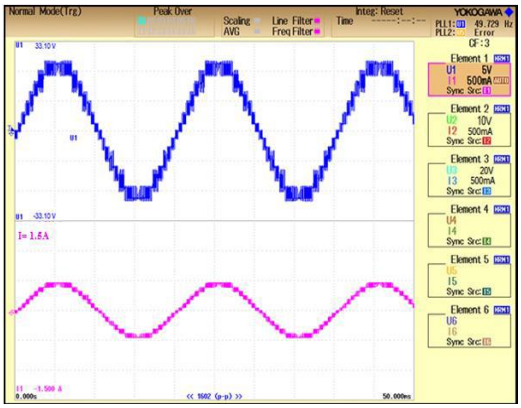

Fig.9. Hardware output current and voltage results of AMLI

Fig.10. shows output voltage and current frequency of the AMLI is found to be 49.729HZ.

Fig.10. Output voltage and current frequency of the AMLI

Fig.11. Hardware THD results of AMLI

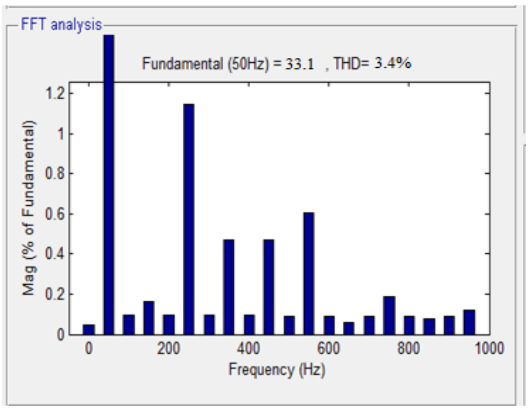

Fig.12. Simulation of THD results of AMLI

VII. CONCLUSION

In this paper asymmetric hybrid 15-level MLI simulation and hardware was effectively designed and implemented. It can be established by suitable modulation technique to reduce the switching frequency. Hybrid modulation system can be used to get the essential output voltage level. The control unit used is the FPGA controller to produce the PWM signals. This 15-level hybrid AMLI contains only 7 switches and removes the capacitors in the clamping diode topology. In order to avoid the power flow problems in the regeneration power loads the inverter was designed. The proposed inverter was essentially implemented and successfully designed. The hardware results are experimentally verified and neatly observed and compared with the simulation results.

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